

MODEL NO.
BL12896AWRNHn\$
VER.07



| FOR MESSRS: | | |
|--------------|--|--|
| ON DATE OF: | | |
| APPROVED BY: | | |

BOLYMIN, INC.

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History of Version

| Version | Contents | Date | Note |
|---------|--|------------|-------|
| 01 | NEW VERSION | 2008/11/17 | SPEC. |
| 02 | Add contrast setting Modify module thickness | 2011/11/9 | |
| 03 | Modify POWER ON/OFF | 2012/05/18 | |
| 04 | UPDATE Quality Assurance · Reliability ADD Precautions for Handling · Precautions for Electrical · Precautions for Storage | 2012/10/02 | M |
| 05 | Modify Cover page | 2012/10/17 | |
| 06 | Modify Quality Assurance | 2013/02/06 | |
| 07 | Modify Optical Characteristics · Interface Pin Function · Drawing · Timing Characteristics · Precautions for Storage | 2017/03/14 | |
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1. Numbering System

| T. IVGII | <u>B</u> | <u>L</u> | 10007 | <u>A</u> | W | <u>R</u> | <u>N</u> | = | <u>H</u> | <u>n\$</u> |
|----------|----------|----------|-------|----------|---|----------|----------|---|----------|------------|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

| 0 | Brand | Bolymin | |
|---|---|---|--|
| 1 | Module Type | C= character type G= graphic type P= TAB/TCP type R=color STN | O= COG type F= COF type L=PLED/OLED |
| 2 | Format | 2002=20 characters, 2 lines 12232= 122 x 32 dots | |
| 3 | Version No. | A type | |
| 4 | LCD Color | W=OLED/White G=STN/gray Y=STN/yellow-green C=color STN | B=blue F=FSTN T=TN |
| 5 | LCD Type | R=positive/reflective P=positive/transflective | M=positive/transmissive N=negative/transmissive |
| 6 | Backlight type/color | L=LED array/ yellow-green H=LED edge/white R=LED array/red G=LED edge/yellow-green F=RGB Q=LED edge/red A=LED edge/amber N=No backlight | D=LED edge/blue E=EL/white B=EL/blue C=CCFL/white Y=LED Bottom/yellow O=LED array/orange K=LED edge/green A=LED edge/amber |
| 7 | CGRAM Font (applied only on character type) | J=English/Japanese Font E=English/European Font G=Chinese(simple) F=Chinese(traditional) | C=English/Cyrillic Font H=English/Hebrew Font A=English/Arabic Font |
| 8 | View Angle/ Operating Temperature | B=Bottom/Normal Temperature H=Bottom/Wide Temperature U=Bottom/Ultra wide Temperature | T=Top/Normal Temperature W=Top/Wide Temperature C=9H/Normal Temperature E=Top/ultra wide temperature |
| 9 | Special Code | n=positive voltage for LCD \$:RoHS | |



2. General Specification

(1) Mechanical Dimension

| Item | Standard Value | Unit |
|--------------------------|------------------|------|
| Number of dots | 128x96 | dots |
| Module dimension (L*W*H) | 33*58.2*1.65 | mm |
| Active area | 26.86*20.14 | mm |
| Dot size | 0.19(W)×0.19(H) | mm |
| Dot pitch | 0.21(W)×0.21 (H) | mm |
| Color | White | |

(2) Controller IC: SSD1329 Controller

(3) Temperature Range

| Operating | DO | -40 ~ +70°C | |
|-----------|----|-------------|--|
| Storage | DU | -40 ~ +85°C | |

3. Absolute Maximum Ratings

| Item | Symbol | Min | Тур | Max | Unit |
|-----------------------|--------|-----|----------|-----|------------------------|
| Operating Temperature | ТОР | -40 | _ | +70 | $^{\circ}\!\mathbb{C}$ |
| Storage Temperature | TST | -40 | _ | +85 | $^{\circ}\!\mathbb{C}$ |
| Input Voltage | VI | _ | _ | VDD | V |
| Operating lift time | | | 10000(1) | | Hrs |
| Operating lift time | | | 13000(2) | | Hrs |
| Operating lift time | | | 16000(3) | | Hrs |

^{*}Note:(A) Under VCC C = 15V, $Ta = 25^{\circ}C$, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 120 cd/m^2 :

Contrast setting: 0x95 Frame rate: 85Hz Duty setting: 1/96

(2) Setting of 100 cd/m^2 :

Contrast setting: 0x72 Frame rate: 85Hz Duty setting: 1/96

(3) Setting of 80 cd/m^2 :

Contrast setting: 0x4F Frame rate: 85Hz Duty setting: 1/96



4. Electrical Characteristics

| Item | Symbol | Condition | Min. | Тур. | Max. | Unit |
|---|--------------------------|-----------|----------------------|------|----------------------|------|
| Supply Voltage For Logic | $ m V_{DD}	ext{-}V_{SS}$ | _ | 2.4 | 3.3 | 3.5 | V |
| Supply Voltage For OLED | Vcc-Vss | _ | 14.5 | 15 | 15.5 | V |
| Input High Vol | $ m V_{IH}$ | _ | $0.8V_{\mathrm{DD}}$ | _ | $V_{ m DD}$ | V |
| Input Low Vol | $V_{\rm IL}$ | _ | 0 | _ | $0.2V_{\mathrm{DD}}$ | V |
| Output High Vol | V_{OH} | _ | $0.9V_{DD}$ | _ | $ m V_{DD}$ | V |
| Output Low Vol. | $V_{ m OL}$ | _ | 0 | _ | $0.1V_{\mathrm{DD}}$ | V |
| Supply Current For Logic (with built-in positive voltage) | I_{DD} | _ | _ | 155 | _ | mA |

5. Optical Characteristics

| Item | Min. | Typ. | Max. | Unit |
|-----------------------|--------|------|------|-------|
| View Angle | 160 | | _ | deg |
| Dark Room contrast | 2000:1 | _ | _ | _ |
| Response Time | | 10 | _ | us |
| Normal mode Luminance | 80 | 100 | | cd/m2 |
| CIE x | 0.26 | 0.30 | 0.34 | |
| CIE y | 0.29 | 0.33 | 0.37 | |



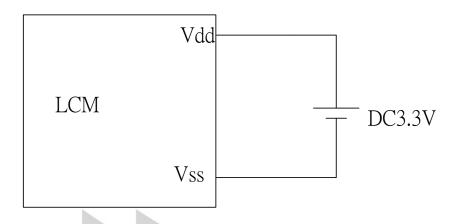
6. Interface Pin Function

| Pin No. | Symbol | Level | Description |
|---------|--------|-------|--------------------------|
| 1 | Vss | 0V | Ground |
| 2 | Vdd | 3.3V | Supply voltage for logic |
| 3 | CS | H/L | Chip select pin |
| 4 | /RES | H/L | Hardware Reset pin |
| 5 | D/C | H/L | H: Data; L: Command. |
| 6 | WR | H/L | write signal pin |
| 7 | RD | H/L | Read signal pin |
| 8 | DB0 | H/L | Data bus line |
| 9 | DB1 | H/L | Data bus line |
| 10 | DB2 | H/L | Data bus line |
| 11 | DB3 | H/L | Data bus line |
| 12 | DB4 | H/L | Data bus line |
| 13 | DB5 | H/L | Data bus line |
| 14 | DB6 | H/L | Data bus line |
| 15 | DB7 | H/L | Data bus line |
| 16 | DISF | H/L | DISF: VCC Voltage ON/OFF |

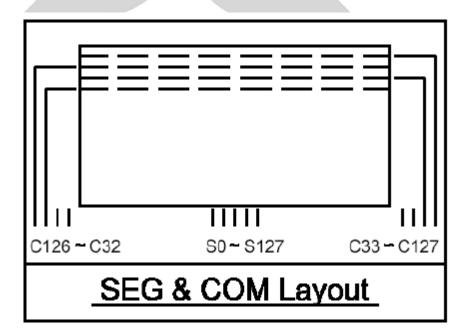


7. Power supply for LCD Module And Panel Layout Diagram

LCM operating on "DC 3.3V" input with built-in positive voltage

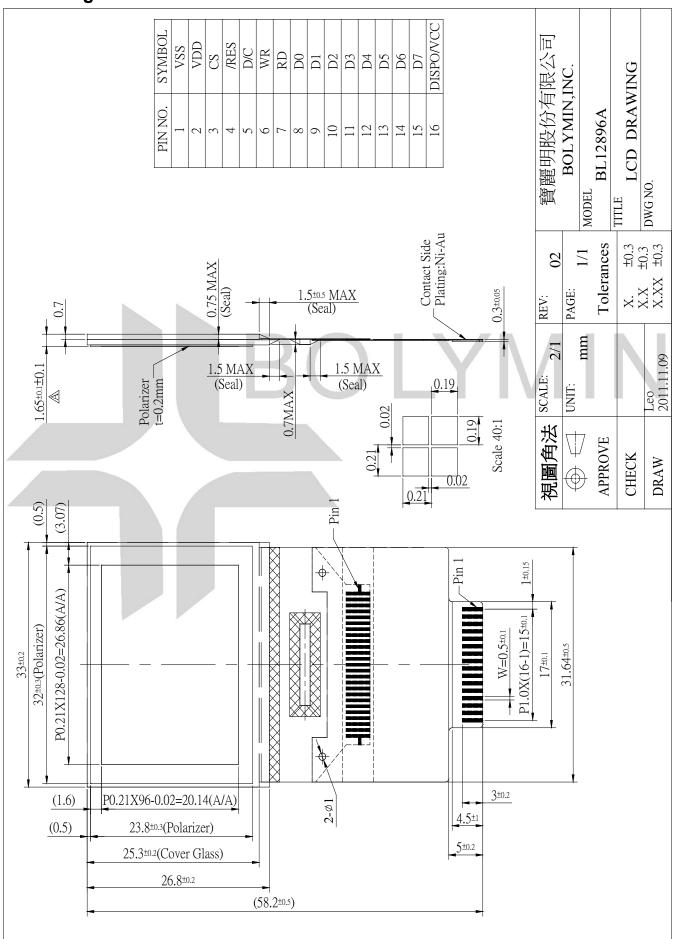


Panel Layout Diagram





8. Drawing

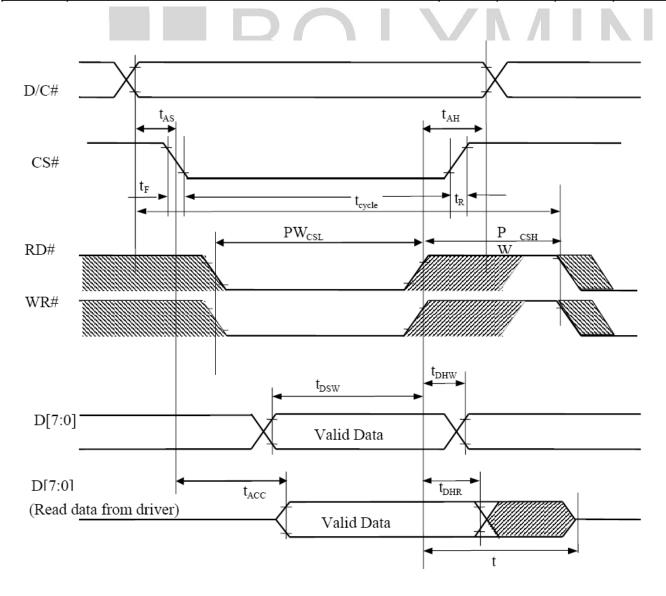




9. SSD1329 controller data 9.1Timing Characteristics

8080 MPU Interface

| Symbol | Parameter | Min | Тур | Max | Unit |
|--------------------|--------------------------------------|-----|-----|-----|------|
| t _{cycle} | Clock Cycle Time | 300 | - | - | ns |
| t_{AS} | Address Setup Time | 0 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| $t_{ m DSW}$ | Write Data Setup Time | 40 | - | - | ns |
| $t_{ m DHW}$ | Write Data Hold Time | 15 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 20 | - | - | ns |
| t _{OH} | Output Disable Time | - | - | 70 | ns |
| t_{ACC} | Access Time | - | - | 140 | ns |
| PW_{CSL} | Chip Select Low Pulse Width (read) | 120 | - | - | ns |
| | Chip Select Low Pulse Width (write) | 60 | | | |
| PW_{CSH} | Chip Select High Pulse Width (read) | 60 | - | - | ns |
| | Chip Select High Pulse Width (write) | 60 | | | |
| t_R | Rise Time | - | - | 15 | ns |
| t_{F} | Fall Time | - | - | 15 | ns |



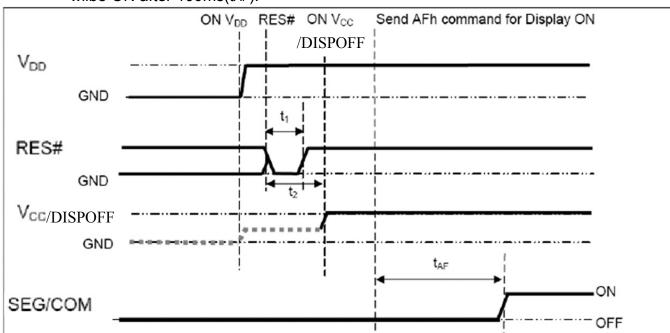


9.2Power ON and OFF sequence

POWER ON / OFF SEQUENCE

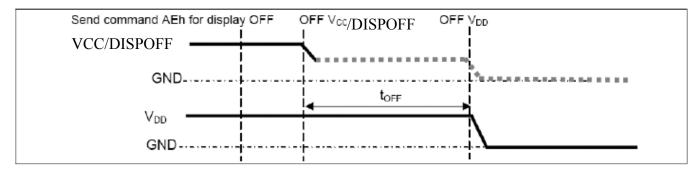
Power ON sequence:

- 1. Power ON VDD.
- 2. After VDD become stable, set RES# pin LOW (logic low) for at least 3us(t1) and then HIGH (logic high).
- 3. After set RES# pin LOW (logic low), wait for at least 3us(t2). Then Power ON VCC.(1)
- 4. After Vcc/DISPOFF become stable, send command AFh for display ON. SEG/COM wilbe ON after 100ms(taf).



Power OFF sequence:

- 1. Send command AEh for display OFF.
- 2. Wait until panel discharges completely.
- 3. Power OFF Vcc. (1), (2)
- 4. Wait for toff. Power OFF VDD. (where Minimum toff=0ms, Typical toff=100ms)



Note:

- (1) Since an ESD protection circuit is connected between VDD and VCC/DISPOFF, VCC/DISPOFF becomes lower than VDD whenever VDD is ON and VCC/DISPOFF is OFF as shown in the dotted line of VCC/DISPOFF in above figures.
- (2) VCC/DISPOFF should be disabled when it is OFF.



9.3 Display Control Instruction

(D/C# = 0, R/W# (WR#) = 0, E (RD#) = 1) unless specific setting is stated

| | amenta Hex | D7 | | D5 | D4 | D3 | D2 | D2 | D0 | Command | Description |
|------------------|------------------------|---------------------|--|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|--|-----------------------------------|---|
| 0 0 0 0 | 15 A[5:0] | 0 * | D6 0 * * | 0 A ₅ B ₅ | 1 A ₄ B ₄ | 0 A ₃ B ₃ | 1 A ₂ B ₂ | 0 A ₁ B ₁ | 1 A ₀ B ₀ | Set Column Address | Description Setup Column start and end address A[5:0]: Start Address, range:00h~3Fh, (POR = 00h) B[5:0]: End Address, range:00h~3Fh, (POR = 3Fh) Please refers to Section 8.10 Graphic Display Data RAM (GDDRAM) for relationship between Column Address setting and GDDRAM structure. |
| 0 0 0 | 75 A[6:0] B[6:0] | O * * | $egin{array}{c} 1 \ A_6 \ B_6 \end{array}$ | 1 A ₅ B ₅ | 1 A ₄ B ₄ | 0 A ₃ B ₃ | 1 A ₂ B ₂ | 0 A ₁ B ₁ | $egin{array}{c} 1 \ A_0 \ B_0 \end{array}$ | Set Row Address | Setup Row start and end address A[6:0]: Start Address, range:00h~7Fh, (POR = 00h) B[6:0]: End Address, range:00h~7Fh, (POR = 7Fh) Please refers to 8.10 Graphic Display Data RAM (GDDRAM) for relationship between Row Address setting and GDDRAM structure. |
| 0 0 | 81 A[7:0] | 1 A ₇ | 0 A ₆ | 0 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 0 A ₁ | 1 A ₀ | Set Contrast Current | A[7:0]: Set Contrast Value, range:0~255, (POR = 80h) |
| 0 0 | 82 A[7:0] | 1 A ₇ | 0 A ₆ | 0 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | $1 \atop A_1$ | 0 A ₀ | Set Second Pre-charge Speed | A[7:1]: Set Second Pre-charge Speed A[7:1] = 00000000b, Second Pre-charge speed = 1 A[7:1] = 0000001b, Second Pre-charge speed = 3 : A[7:1] = 1111111b, Second Pre-charge speed = 255 The RESET value of A[7:1] depends on the value of the contrast current (81h) and is equal to: 2*81h A[7:0] +1 (maximum 7Fh) A[0] = 0, Disable doubling the Second Pre-charge speed (POR) A[0] = 1, Enable doubling the Second Pre-charge speed Please refer to Figure 10-3 for the illustration of difference Second Pre-charge speed settings. |
| 0 | 90 A[7:0] | 1 ** | 0 ** | 0 A ₅ | 1 A ₄ | 0 * | 0 ** | 0 A ₁ | 0 A ₀ | Set Master Icon Control | A[1:0]: Icon control A[1:0] = 00b, Icon RESET to normal display (POR) A[1:0] = 01b, Icon All ON (without altering icon ON / OFF register) A[1:0] = 10b, Icon All OFF (without altering icon ON/ OFF register) A[4] = 0b, Disable icon display (POR) A[4] = 1b, Enable icon display A[5] = 0b, Disable V _{ICON} charge pump circuit (POR) A[5] = 1b, Enable V _{ICON} charge pump circuit |



| Fune | damenta | l Cor | nmano | l Tabl | e | | | | | | |
|-----------|--|---------------------|---|---|---|---|---|---|---|---|--|
| | # Hex | D 7 | D6 | D5 | D4 | D3 | D2 | D2 | D0 | Command | Description |
| 0 | 91 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | | A[7:0]: Set Icon current |
| 0 | A[7:0] | A ₇ | A_6 | \mathbf{A}_{5} | A_4 | \mathbf{A}_3 | \mathbf{A}_2 | A_1 | A_0 | Set Icon Current Range | A[7:0] = 00h, max icon current = 0.0uA A[7:0] = 01h, max icon current = 0.5uA A[7:0] = 02h, max icon current = 1.0uA A[7:0] = 03h, max icon current = 1.5uA A[7:0] = 04h, max icon current = 2.0uA A[7:0] = FCh, max icon current = 126.0uA A[7:0] = FDh, max icon current = 126.5uA A[7:0] = FEh, max icon current = 127.0uA A[7:0] = FFh, max icon current = 127.5uA (POR) Note (1) The larger is the icon current range, the better the uniformity is. |
| 0 0 0 0 0 | 92 A0[6:0] A1[6:0] A62[6:0] A63[6:0] | | 0 A0 ₆ A1 ₆ A62 ₆ A63 ₆ | 0 A0 ₅ A1 ₅ A62 ₅ A63 ₅ | 1 A0 ₄ A1 ₄ A62 ₄ A63 ₄ | 0 A0 ₃ A1 ₃ A62 ₃ A63 ₃ | 0 A0 ₂ A1 ₂ A62 ₂ A63 ₂ | 1 A0 ₁ A1 ₁ A62 ₁ A63 ₁ | 0 A0 ₀ A1 ₀ A62 ₀ A63 ₀ | Set Individual Icon Current | Set each Icon current by the formula: (AN[6:0] / 127) x max icon current, where the max icon current is defined by the command "Set icon current range" 91h and N=0~63. e.g. Icon Current of ICS0 = (A0[6:0]/127) x max icon current. A0[6:0]: icon current for ICS0, range: 00h~7Fh A1[6:0]: icon current for ICS1, range: 00h~7Fh A63[6:0]: icon current for ICS62, range: 00h~7Fh A64[6:0]: icon current for ICS63, range: 00h~7Fh Note (1) All 64 levels (1 level for each ICS signals) of icon current must be entered to operate this command properly. (2) The icon current of the unselected icon pins must be set to zero by this command. |
| 0 | 93 A[7:0] | 1 A ₇ | 0 A ₆ | 0 A ₅ | 1 A ₄ | 0 A ₃ | 0 A ₂ | 1 A ₁ | 1 A ₀ | Set Individual Icon ON / OFF Register | Individual icon selection: A[5:0]: select one of the 64 icons from ICS0 ~ ICS63 A[7:6] = 00b, turn OFF selected icon A[7:6] = 01b, turn ON selected icon A[7:6] = 11b, blink selected icon e.g A[7:0] = 01000000b, turn ON icon ICS0 A[7:0] = 00111111b, turn OFF icon ICS63 |
| 0 0 | 94 A[7:6] | 1 A ₇ | 0 A ₆ | 0 * | 1 ** | 0 ** | 1 ** | 0 ** | 0 * | Set Icon ON / OFF Registers | A[7:6]: Icon register A[7:6] = 00b, turn OFF all icon A[7:6] = 01b, turn ON all icon A[7:6] = 11b, blink all icons |



| | amenta Hex | D7 | D6 | D5 | D4 | D3 | D2 | D2 | D0 | Command | Description |
|------------|---------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|----------------------------|--|
| <i>C</i> # | Constant | 180 | r Chara | _ | Ta a | _ | 20 | _ | 100 | Command | A[2:0]: Set Icon blinking cycle: |
| | 95 A[7:0] | 1 | O str | 0 A ₅ | 1 A ₄ | O *** | A_2 | 0 A ₁ | A_0 | Set Icon Blinking Cycle | 000b 0.25sec 001b 0.50sec 010b 0.75sec 011b 1.00sec (POR) 100b 1.25sec 101b 1.50sec 110b 1.75sec 111b 2.00sec |
|)) | 96 A[7:0] | 1 A ₇ | 0 A ₆ | 0 A ₅ | 1 A ₄ | O ** | 1 A ₂ | 1 A ₁ | 0 A ₀ | Set Icon Duty | A[2:0]: Set icon AC drive 000b DC drive (POR) 001b 63 / 64 duty ratio 010b 62 / 64 duty ratio 011b 61 / 64 duty ratio 100b 60 / 64 duty ratio 101b 59 / 64 duty ratio 110b 58 / 64 duty ratio 111b 57 / 64 duty ratio A[7:4]: Set icon frame frequency Note (1) Icon frame frequency must NOT be set to 0000b |
| | A0 A[7:0] | 1 A ₇ | 0 A ₆ | 1 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 0 A ₁ | 0 A ₀ | Set Re-map | Re-map setting in Graphic Display Data RAM (GDDRAM) A[7:0]: Remap (POR = 00h) A[0] = 0b, Disable Column Address Re-map (POR) A[0] = 1b, Enable Column Address Re-map A[1] = 0b, Disable Nibble Re-map (POR) A[1] = 1b, Enable Nibble Re-map A[2] = 0b, Enable Horizontal Address Increment (POR A[2] = 1b, Enable Vertical Address Increment A[4] = 0b, Disable COM Re-map (POR) A[4] = 1b, Enable COM Re-map A[6] = 0b, Disable COM Split Odd Even (POR) A[6] = 1b, Enable COM Split Odd Even |



| D/C# | amenta Hev | D7 | D6 | D5 | D4 | D3 | D2 | D2 | D0 | Command | Description |
|------------------|----------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|-------------------------------|--|
| | A1 | 1 | 0 | 100 | 0 | 0 | 0 | 0 | Fig. | Command | A[6:0]: Vertical scroll by setting the starting address of |
| 0 0 | A[7:0] | * | \mathbf{A}_{6} | 1 A ₅ | A ₄ | A ₃ | A ₂ | A_1 | A_0 | Set Display Start Line | display RAM from $0 \sim 127$ (POR = 00h) |
| 0 | A2 A[7:0] | 1 | 0 A ₆ | 1 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 1 A ₁ | 0 A ₀ | Set Display Offset | A[6:0]: Set vertical offset by COM from 0 ~ 127 (POR = 00h) e.g. Set A[6:0] to 010000b to move COM16 towards COM0 direction for 16 row |
| 0 0 0 0 | A4 A5 A6 A7 | 1 1 1 1 | 0 0 0 0 | 1 1 1 1 | 0 0 0 0 | 0 0 0 0 | 1 1 1 1 1 | 0 0 1 1 | 0 1 0 1 | Set Display Mode | A4: Normal display (POR) A5: All ON (All pixels have gray scale of 15, GS15) A6: All OFF (All pixels have gray scale of 0, GS0) A7: Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13,) |
| 0 | A8 A[6:0] | O ** | 0 A ₆ | 0 A ₅ | 1 A ₄ | 0 A ₃ | 1 A ₂ | 0 A ₁ | 1 A ₀ | Set MUX Ratio | A[6:0]: Set MUX ratio from 16MUX \sim 128MUX: A[6:0] = 15 represents 16MUX A[6:0] = 16 represents 17MUX : A[6:0] = 126 represents 127MUX A[6:0] = 127 represents 128MUX (POR) It should be noted that A[6:0]=0 \sim 14 is not allowed. |
| 0 | AE AF | 1 | 0 | 1 | 0 | 1 | 1 1 | 1 | 0 | Set Sleep mode ON / OFF | A[0] = 0b, Sleep mode ON (The display is OFF) A[0] = 1b, Sleep mode OFF (The display is ON) |
| 0 | B1 A[7:0] | 1 A ₇ | 0 A ₆ | 1 A ₅ | 1 A ₄ | 0 A ₃ | 0 A ₂ | 0 A ₁ | 1 A ₀ | Set Phase Length | A[7:0]: RESET and first pre-charge phase length (POR=53h) A[3:0]: Phase 1 period of 1~16 DCLK's (POR=3h) e.g. A[3:0] = 1111b, 16 DCLK Clock A[7:4]: Phase 2 period of 1~16 DCLK's (POR=5h) e.g. A[7:4] = 1111b, 16 DCLK Clocks |
| 0 | B2 A[6:0] | 1 | 0 A ₆ | 1 A ₅ | 1 A ₄ | 0 A ₃ | 0 A ₂ | 1 A ₁ | 0 A ₀ | Set Frame Frequency | Set the frame frequency of the matrix display A[6:0]:Total number of DCLK's per row. Ranging from 14h to 4Eh DCLK's (POR = 23h) Then the frame Frequency = DCLK freq /A[6:0]. |



| a transmission residence | amenta | | and the second second | | 30 | | | | | _ | | |
|--------------------------|--------------------------------------|---------------------|-----------------------|---|-------------------------------------|---|---|---|---------------------|--|--|--|
| D/C# | | D 7 | D6 | D 5 | D4 | D3 | D2 | D2 | D0 | Command | Description | |
| 0 | B3 A[7:0] | 1 A ₇ | 0 A ₆ | 1 A ₅ | 1 A ₄ | 0 A ₃ | 0 A_2 | 1 A ₁ | A_0 | Set Front Clock Divider /Oscillator Frequency | A[3:0]: Define divide ratio (D) of display clock (DCLK Divide ratio=A[3:0]+1 (POR is 0000b, i.e. divide ratio = 1) A[7:4]: Set the Oscillator Frequency, F _{OSC} . Oscillator Frequency increases with the value of A[7:4] and vice versa. Range:0h~Fh (POR= 0h represents 500KHz, typical step value: 4% of previous value) | |
| 0 | B7 | 1.00 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | Set Default Gray Scale Table | The default gray scale table is set in unit of DCLKs as follow: GS1 level Pulse width = 2 DCLKs GS2 level Pulse width = 4 DCLKs GS3 level Pulse width = 6 DCLKs GS13 level Pulse width = 26 DCLKs GS14 level Pulse width = 28 DCLKs GS15 level Pulse width = 30 DCLKs | |
| 0 0 0 0 | B8 A1[5:0] A2[5:0] A14[5:0] A15[5:0] | 1 | 0 * * * * * * | 1 A1 ₅ A2 ₅ A1 ₄₅ A15 ₅ | 1 A14 A24 A144 A154 | 1 A1 ₃ A2 ₃ A14 ₃ A15 ₃ | 0 A1 ₂ A2 ₂ A14 ₂ A15 ₂ | 0 A1 ₁ A2 ₁ A14 ₁ A15 ₁ | O A10 A20 A140 A150 | Look Up Table for Gray Scale Pulse width | Set gray scale (GS1~GS15) pulse width in unit of DCLKs. A1[5:0], value for GS1 level Pulse width A2[5:0], value for GS2 level Pulse width A14[5:0], value for GS14 level Pulse width A15[5:0], value for GS15 level Pulse width Note (I) The pulse width value of GS1, GS2,, GS15 should not be equal. i.e. 0 <gs1<gs2 <gs15<="" td=""></gs1<gs2> | |
| 0 | BB A[3:0] | 1 ** | 0 ** | 1 ** | 1 ** | 1 A ₃ | 0 A ₂ | 1 A ₁ | 1 A ₀ | Set Second Pre-charge Period | A[3:0]: Set Second pre-charge period 0000b | |



| D/C# | Hex | D 7 | D6 | D5 | D4 | D3 | D2 | D2 | $\mathbf{D0}$ | Command | Description | |
|------|--------------|------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---|---|--|
| 0 | BC A[5:0] | * | O ** | 1 A ₅ | 1 A ₄ | 1 A ₃ | 1 A ₂ | 0 A ₁ | 0 A ₀ | Set First Precharge voltage, V_{P} | $A[5:0]: Set First Pre-charge voltage \\ 000000b & 0.30 \times V_{CC} \\ 000001b & 0.31 \times V_{CC} \\ & \\ 001111b & 0.45 \times V_{CC} \ (POR) \\ & \\ 011111b & 0.63 \times V_{CC} \\ 1xxxxxb & 1.00 \times V_{CC} \ or \ connect \ to \ V_{COMH} \ if \\ V_{CC} > V_{COMH} \\ \\ \end{tabular}$ | |
| 0 | BE A[6:0] | 1 | 0 A ₆ | 1 A ₅ | 1 A ₄ | 1 A ₃ | 1 A ₂ | 1 A ₁ | 0 A ₀ | Set $V_{	extsf{COMH}}$ | $ \begin{array}{cccccccccccccccccccccccccccccccccccc$ | |
| 0 | E3 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | NOP | Command for No Operation | |
| 0 | FD A[2] | 1 0 | 1 0 | 1 0 | 1 | 1 0 | 1 A ₂ | 0 | 1 0 | Set Command Lock | A[2]: MCU protection status (POR = 12h) A[2] = 0h, disable locking the MCU from entering command (POR) A[2] = 1h, enable locking the MCU from entering command Note (1) Locking prohibits all commands and memory access | |

Note
(1) "**" stands for "Don't care".
(2) POR stands for Power On Reset.



10 Quality Assurance

10.1 Inspection conditions

1. The inspection and meaurement are performed under the following conditions,

2. unless otherwise specified.

3. Temperature: 25±5°C

4. Humidity: 50±10%R.H.

5. Distance between the panel and eyes of the inspector≥30cm

10.2 Inspection Parameters

| Severity | Inspection Item | Defect | Remark | | |
|----------|-----------------|------------------------------------|------------|--|--|
| | | (1) Non-displaying | | | |
| | 1. Panel | (2) Line defects | | | |
| | i. Failei | (3) Malfunction | | | |
| Major | 160 | (4) Glass cracked | | | |
| Defect | 2. Film | (1) Film dimension out of | Can not be | | |
| | 2.1 11111 | specification | assembled | | |
| | 3. Dimension | (1) Outline dimension out | / / | | |
| | o. Diricision | of specification | | | |
| | | (1) Glass scratch | VIII | | |
| | 1. Panel | (2) Glass cutting NG | | | |
| | | (3) Glass chip | | | |
| | | (1) Polarizer scratch | Appearance | | |
| Minor | 2. Polarizer | 2. Polarizer (2) Stains on surface | | | |
| Defect | | (3) Polarizer bubbles | defect | | |
| | 2. Displaying | (1) Dim spot · | uelect | | |
| | 3. Displaying | Bright spot \ dust | | | |
| | 4. Film | (1) Damage (2) Foreign material | | | |



| | | | | | " | |
|------------------------|---|--|--------------------------------|--------------------|-------|--|
| Description | | Criterion | | | | |
| 1. Glass scratch | Width (mm) W W≤0.03 0.03< W≤0.05 | Length (mm) L Ignore L≦3 | numbe piec permi Igno | es itted ore | Minor | |
| | 0.05< W | | Nor | | | |
| | beyond A.A. | | Igno | ore | | |
| | | | | | | |
| 2. Polarizer bubble | Size $ \begin{array}{c} \varphi \leq 0.2 \\ 0.2 < \varphi \leq 0.5 \\ 0.5 < \varphi \\ \text{beyond A.A.} \end{array} $ | number pieces per Ignor 2 0 Ignor | mitted e | nitted e | | |
| | | 1 | | | | |
| | average | number | of | | VI | |
| | D ≦0.1 | Ignor | е | | | |
| 3. Dimming spot \ | 0.1 < D ≤0.15 | | | | | |
| Lighting spot · | 0.15< D ≤0.2 | _ | | | Minor | |
| Dust | 0.2 < D | 0 Ignor | _ | | | |
| | beyond A.A. D=(long diamete | | | | | |
| | Pixel off is not allo | | | | | |



10.3 WARRANTY POLICY

Bolymin . Will provide one-year warranty for the products only if under specification operating conditions.

If there are functional defects found during the period of warranty, the defective products would be replaced on a one-to-one basis.

Bolymin would not be responsible for any direct/indirect liabilities consequential to any parties.

10.4 MTBF

10.4.1 .MTBF based on specific test condition is 13K hours.

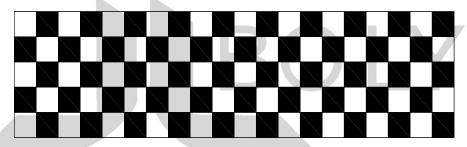
10.4.2 Test Condition:

10.4.2.1 Supply Voltage: Vcc=15.0V

10.4.2.2 Luminance: 100 cd/m2

10.4.2.3 Operation temperature and humidity:25 °C and 50%RH

10.4.2.4 Run-Patterns:



10.4.3 Test Criteria:

Luminace has decayed to less than 50% of the initial measured luminance.



11.Reliability

■Content of Reliability Test

| NO. | Items. | Specification | Applicable Standard |
|-----|---|---|------------------------|
| 1 | High temp. (Non-operation) | 85°C, 240hrs | |
| 2 | High temp. (Operation) | 70°C, 120hrs | |
| 3 | Low temp. (Operation) | -40°C, 120hrs | |
| 4 | High temp. / High. humidity (Operation) | 65°C, 90%RH, 120hrs | |
| 5 | Thermal shock(Non-operation) | -40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles. | |
| 6 | Vibration | Frequency: 5~50HZ, 0.5G Scan rate: 1 oct/min Time: 2 hrs/axis Test axis: X, Y, Z | |

Test and measurement conditions

- 1. All measurements shall not be started until the specimens attain to temperature stability.
- 2. All-pixels-on is used as operation test pattern.
- 3. The degradation of Polarizer are ignored for item 1 & 4 & 5.

Criteria

- 1. The function test is OK.
- 2. No observable defects.
- 3. Luminance: >50% of initial value.
- 4. Current consumption: within ±50% of initial value.

Reliability Test

Bolymin only guarantees the reliability of the panel under the test conditions and durations listed in the specification, and is not responsible for any test results that are conducted using more stringent conditions and/or with lengthened durations. Also, when the testing the panel in a chamber or oven, make sure they won't produce any condensation on the panel, especially on the electrical leads, before lighting on the panel to see if it passes the test. Also the panel should rest for about an hour at room temperature and pressure before the measurement, as indicated in the specification. Be aware that one should use fresh panel for each of the reliability test items listed in the specification, in other words, don't use the panels that were tested for subsequent tests.



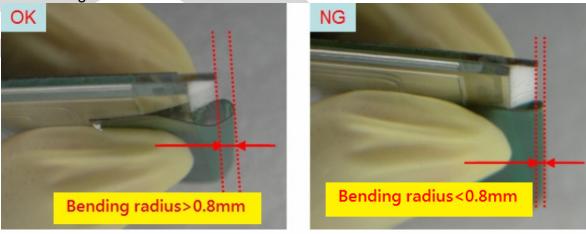
12. Precautions for Handling

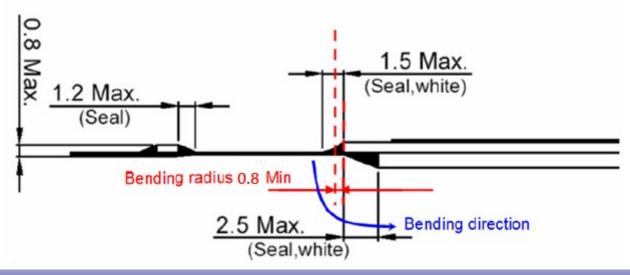
- 12.1 When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.
- 12.2 The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a height.
- 12.3 The OLED module is an electronic component and is subject to damage caused by Electro Static

Discharge (ESD) and hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Also, ground the tools being used for panel assembly and make sure the working environment is not too dry to cause ESD problems. (See the photos below).



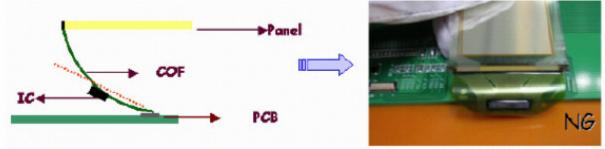
12.4 Please do not bend the film near the substrate glass.(this could cause film peeling and COF damage) and the peeling strength about 600g/cm, the bending <20times and the bending radius :R>0.8mm



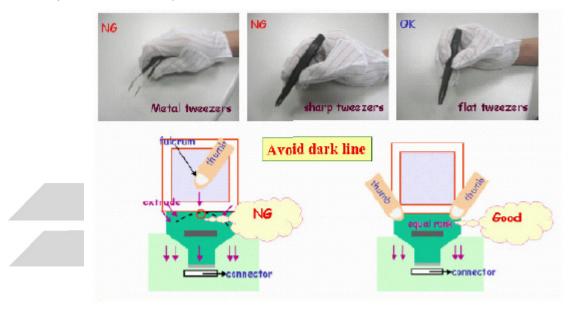




12.5 Avoid bending the film at IC bonding area.(>1.5mm)(this could damage the ILB bonding)



12.6 Use both thumbs to insert COF into the connector when assembling the panel. See the photo on the far right below for correct insertion of the film into the connector (one-handed insertion exerts uneven force on the film and could cause its breakage, photo on the left)



12.7 Do not wipe the pin of film with the dry or hard materials that will damage the surface. When cleaning the display surface, use soft cloth solvent and wipe gently (Recommend solvent: IPA, alcohol), and do not wipe the display with dry or hard materials that will damage the polarizer surface and do not use the solvent like: Water, Acetone, Aromatic



13. Precautions for Electrical

13.1.Design using the settings in the specification

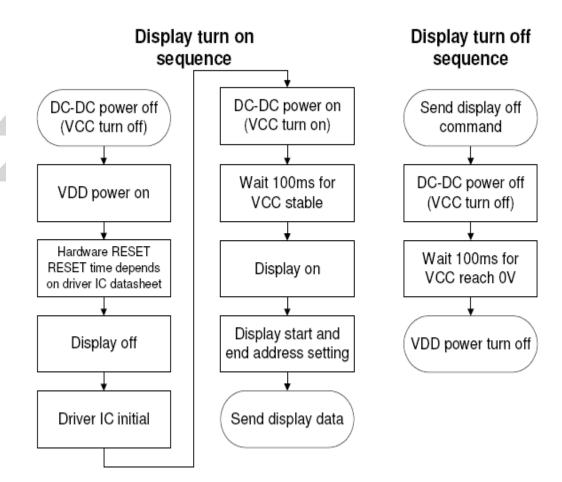
It is extremely important to design and operate the panel using the settings listed in the specification. This includes voltage, current, frame rate, duty cycle... etc. Operation of the OLED outside the specified range in the specification should be entirely avoided to ensure proper operation of the OLED.

13.2. Maximum Ratings

To ensure proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

13.3 Power on/off procedure

Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, could cause OLED panel malfunctioning.



13.4 Power savings

To save power consumption of the OLED, one can use partial display or sleep mode when the panel is not fully activated. Also, if possible, make maximum use of black background to save power. The OLED is a self-luminous device, and a particular pixel cluster or image can be lit on via software control, so power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode.



The power consumption is almost in direct proportion to the brightness of the panel, and also in direct proportion to the number of pixels lit on the panel, so the customer can save the power by the use of black background and Sleeping Mode. One benefit from using these design schemes is the extension of the OLED lifetime.

13.5 Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. The time when image sticking happens depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following three strategies to minimize image sticking

- 13.5.1Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.
- 13.5.2Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays
- 13.5.3If in the reliability test when a static logo is used, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns



14. Precautions for Storage

Although the storage conditions and guarantee period are indicated in the specification, it is advisable to store the packed cartons or packages at $23^{\circ}\pm5^{\circ}$,55%±10%RH(Note A), Do not store the OLED module under direct sunlight or UV light and for best panel performance. The constant working OLED display module decays slower than the module that is not working. And it's better to use the module on the field within one month after unpacking the package.

Note (A):

Vacuum Packaging

Desiccant x 2







Humidity indicator card

As the humidity increases, the chemically impregnated spots change from a brown color (DRY) to a blue color (HUMID).

